REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 7-15, and 21-23 are pending in the present application. Claims 1 and 7 have been amended by the present amendment.

In the outstanding Office Action, Claims 1 and 9 were rejected under 35 U.S.C. § 102(b) as anticipated by JP 04-197126 (hereinafter JP '126); Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP 10-199882 (hereinafter JP '882) in view of Lee; Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP '882 in view of Ma; and Claims 10-12 and 21-23 were allowed.

Applicant thanks the Examiner for the indication of allowable subject matter.

Claims 1 and 9 were rejected under 35 U.S.C. § 102(b) as anticipated by JP '126. This rejection is respectfully traversed.

Amended Claim 1 finds support in Figure 7, and is directed to a semiconductor device having interlayer insulating films, conductive interconnections provided in a plurality of layers, conductive dummy interconnections and a conductive dummy plug. Further, the conductive dummy interconnections are disposed so that each conductive dummy interconnection is formed in a layer of the plurality of layers with at least one conductive interconnection.

In a non-limiting example, Figure 7 shows the interlayer insulating films 4, the conductive interconnections 8a-8g and the conductive dummy interconnections 9a-9b.

The present invention addresses a problem of a noise caused by dummy interconnections in floating state that have no direct involvement in a circuit function and are provided in multi-layered interlayer insulating films along with conductive interconnections

to reduce a level difference. The present invention advantageously provides a solution to this problem by connecting multi-layer dummy interconnections with plugs that are not directly involved in the circuit function and applying an electrical potential to the multi-layer dummy interconnections, so to reduce the noise which occurs in the vicinity of the dummy interconnections.

As recognized in the outstanding Office Action at page 2, item 2, JP '126 discloses a semiconductor device having a conductive dummy interconnection 16 which is formed in a layer which does not have any conductive interconnections 12 or 20. Therefore, JP '126 does not teach or disclose (1) providing conductive dummy interconnections so that each conductive dummy interconnection is formed in a layer of a plurality of layers with at least one conductive interconnection and (2) providing dummy lines to improve a flatness of interlayer insulating films and lines. Also, JP '126 does not identify a noise problem caused by floating dummy lines.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP '882 in view of Lee. This rejection is respectfully traversed.

In Figure 2 of JP '882 and as recognized in the outstanding Office Action at page 3, item 4, a conductive dummy interconnection 12 is formed in a layer which does not have at least one conductive interconnection 3, 5, 7 or 9, as recited in Claim 1. In addition, JP '882 does not teach or suggest applying an electrical potential to dummy lines for reducing a noise, as in the claimed invention.

Lee is asserted for its teaching of having dummy lines connected to a potential power supply line. However, Lee does not teach or suggest what is also lacking in JP '882, namely,

conductive dummy interconnections formed so that each conductive dummy interconnection is formed in a layer of a plurality of layers with at least one conductive interconnection.

Further, Lee is related to reducing level differences in interlayer insulating films by use of dummy lines. Thus, Lee does not teach or suggest a noise caused by the dummy lines in floating state. In addition, Lee states the dummy lines 44, in Figure 12, "can be left floating, or can be grounded with line 60," and there is no disclosure of the necessity that lines 60 are connected to dummy lines 44 or 22.[1]

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP '882 in view of Ma. This rejection is respectfully traversed.

The device in JP '882 has been discussed above.

Ma is asserted for its teaching of forming a dummy interconnection surrounding a signal interconnection line 90 and connecting to a potential power supply line V_{ss}. Further, Ma discloses lines 102, 104, 106 and 108 surrounding and isolating line 90, for example in Figure 5. However, Ma does not teach or suggest what is also lacking in JP '882, namely, conductive dummy interconnections formed so that each conductive dummy interconnection is formed in a layer of a plurality of layers with at least one conductive interconnection and dummy lines.

Therefore, it is respectfully submitted the combination of JP '882 in view of Ma does not achieve the same advantages as the present invention.

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[1]Lee, column 5, lines 60-62.

In addition, the abstract of the disclosure has been amended to conform with standard U.S. patent practice.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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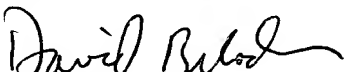

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IN THE CLAIMS

Please amend Claims 1 and 7 as follows:

--1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films;

conductive dummy interconnections provided in the [same] plurality of layers [as said interconnections in two or more layers included in] so that each conductive dummy interconnection is formed in a layer of said plurality of layers with at least one conductive interconnection; and

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

7. (Amended) The semiconductor device according to claim 1, wherein said dummy interconnections are provided to sandwich an interconnection part included in said interconnections in at least one [of said two or more] layer of said plurality of layers.--

IN THE ABSTRACT

Please amend the abstract to read as follows:

--[An object is to reduce] A semiconductor device which reduces a noise superimposed upon a signal carried on an interconnection or cross-talk. Dummy interconnections [(9, 21 and 25)] are formed in the same layers respectively as interconnections [(8, 19 and 28)] formed in a plurality of layers. The dummy interconnections [(9, 21 and 25)] are connected through dummy plugs [(22 and 26)]. At least the dummy interconnections [(9a, 21a, 21c and 25a)] and the dummy plugs [(22a, 26a and 26c)] are fixed at a ground potential.--